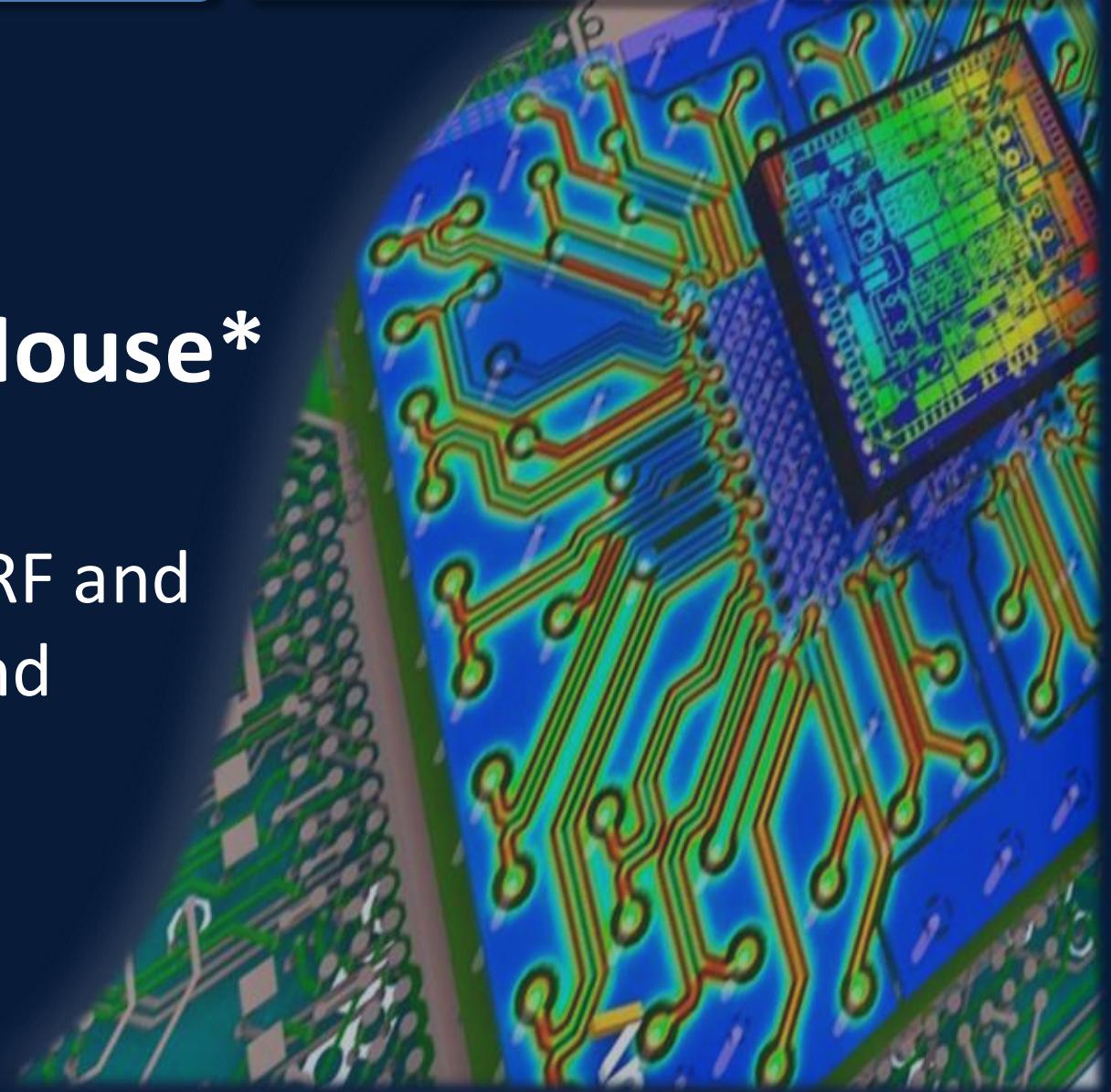




Integrated Circuit Design House*

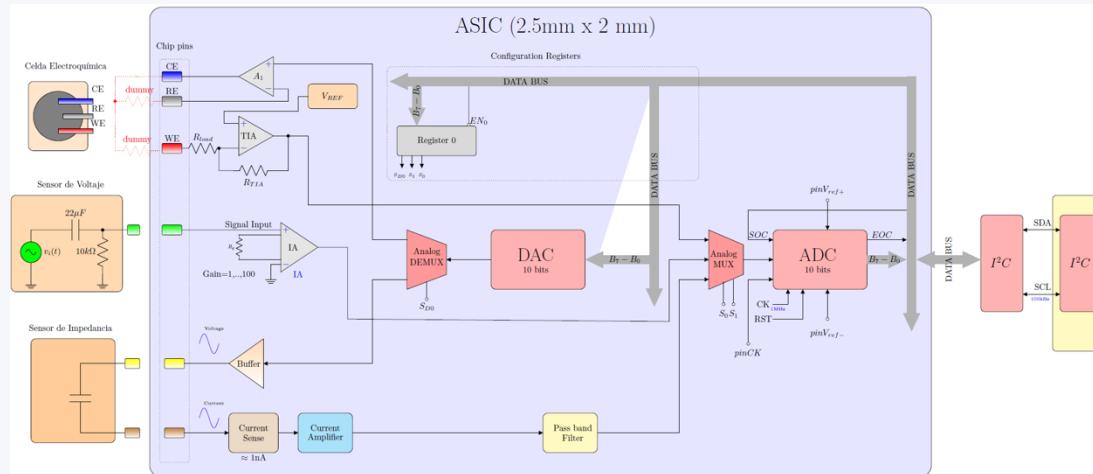
We focus on analog, mixed-mode, RF and digital design for the automotive and medical equipment, and household appliances.

* With the support of the State Governments of Jalisco, Puebla, and Sonora.

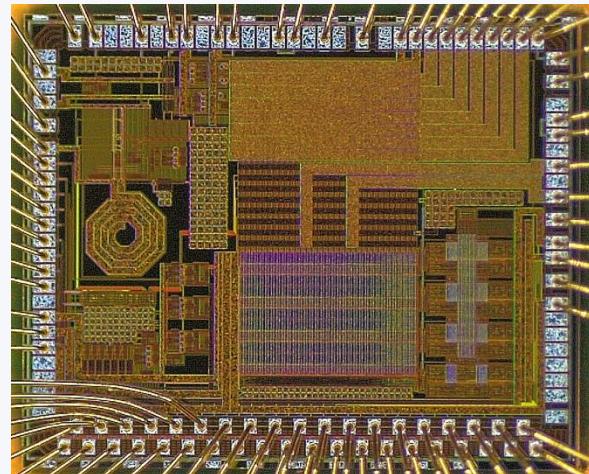


From the concept to the silicon chip and testing

Concept and client specs



Layout IC design & simulation



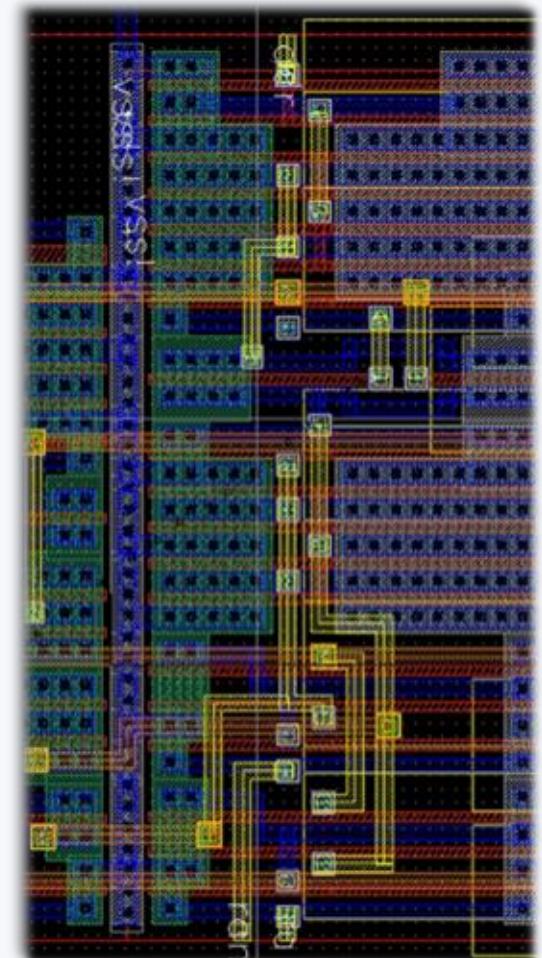
Prototyping & testing



We work under the concept of fabless and tape out for manufacture in 180 nm, 65 nm, 22 nm, or 16 nm

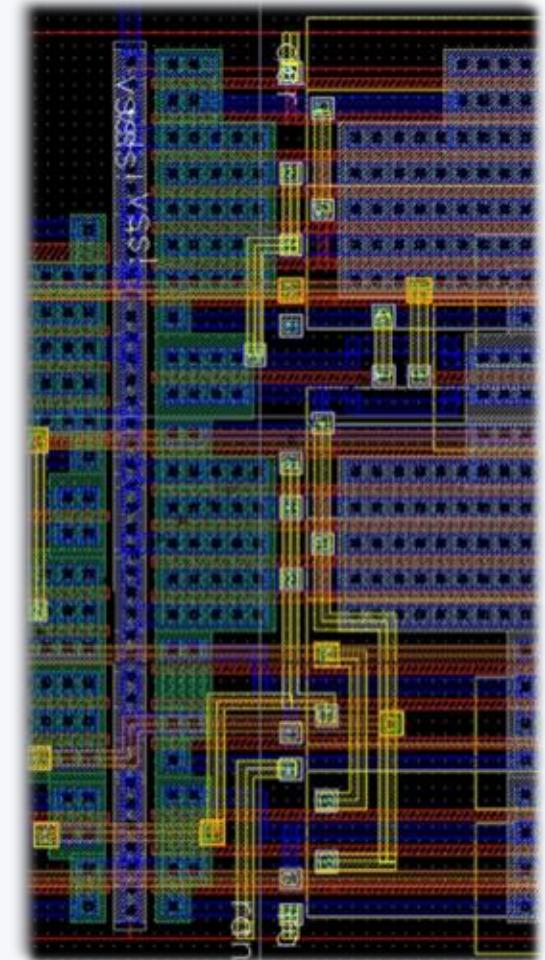
Who we are?

- A group of designees with more than 20 years of experience recruited from the academia and industry.
- We are located in Mexico with offices in the states of Puebla, Jalisco, and Sonora.
- We are aimed at foster the semiconductors supply chain in Mexico in support of the North American market.
- We train designers through a specialized 6-months program with hands on design tools, and fabrication of a test chip.
- We look for collaboration for co-design of integrated circuits.

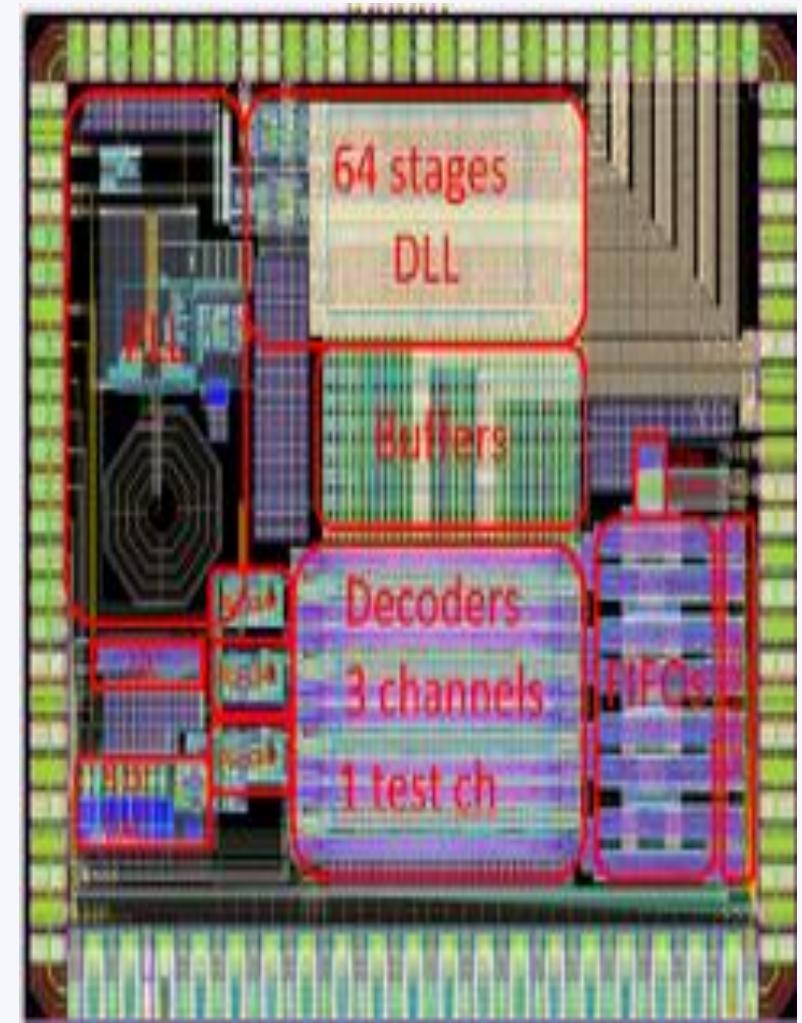
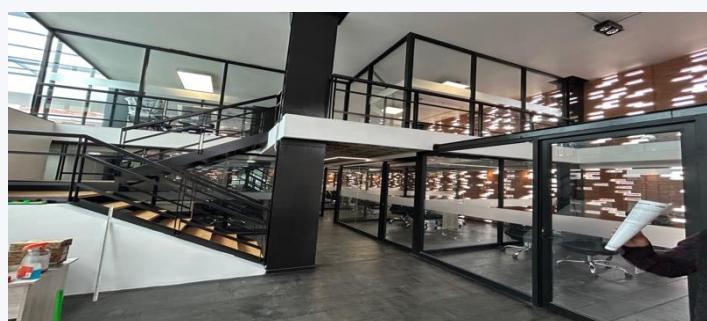
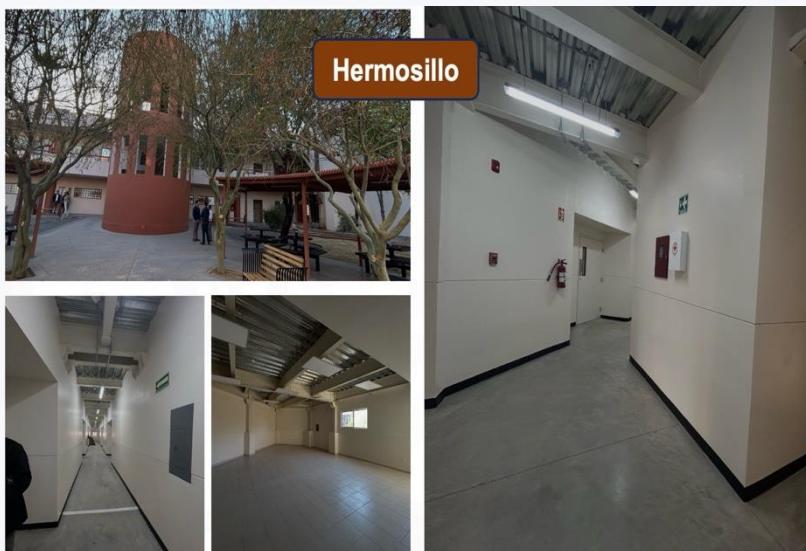


We aim at

- Setting up a 100 IC designers design house by 2027.
- Strengtegning the Academia-Industry collaboration.
- Achieving economic self-sustainability by 2028.
- Promote the creation of other design houses.
- Establish the conditions for the installation of a semiconductor factory by 2030.



Our offices in Puebla, Jalisco, and Sonora.



Leadership Team & Contact

Credible leadership and an execution-focused technical bench



Dr. Edmundo Gutiérrez General head

PhD, Catholic University of Leuven, Belgium, 1993.

<https://scholar.google.com/citations?hl=es&user=eRQRMb8AAAAJ>

A technical group of 15 designers with a PhD in circuit synthesis and design, analog and digital signal processing, IoT security, analog/RF and mixed signal, low-power systems, 5G and wireless communications, ASIC, SoC design, FPGA embedded systems, readout circuits, scientific instrument development, Analog-to-Digital and Digital-to-Analog converters, medical and environmental oriented applications, graphic interfaces for ASIC controlling, design and characterization of image arrays, ESD protection, signal integrity, and reliability at room and cryogenic temperatures. We have designed in different technologies, such as 16 nm, 65 nm, and 180 nm CMOS, and tested 14nm FinFET technology for reliability modeling.

Dr. Edmundo Gutiérrez

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Dr. Alejandro Bautista

PhD, INAOE, Puebla, Mexico
Technical director, Puebla, 2018

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Dr. Ramón Parra

Technical director, Jalisco
PhD, CINVESTAV, Mexico, 2003

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Dr. Roberto Gómez

Technical director, Sonora
PhD, INAOE, Puebla, 2007.

<https://scholar.google.com/citations?user=O5yE45MAAAJ&hl=es>