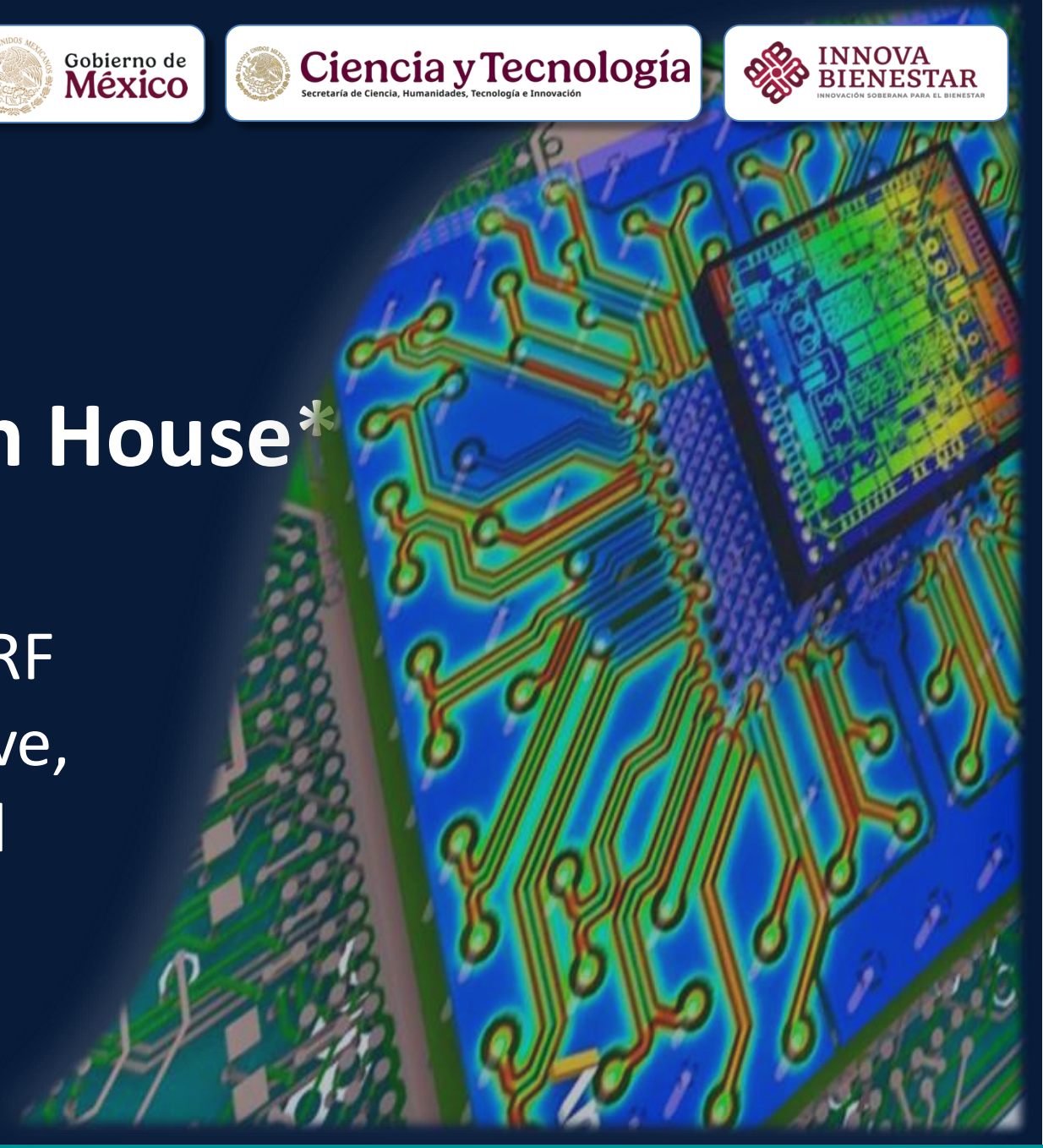
Kutsari Semiconductors ®

An Integrated Circuit Design House*

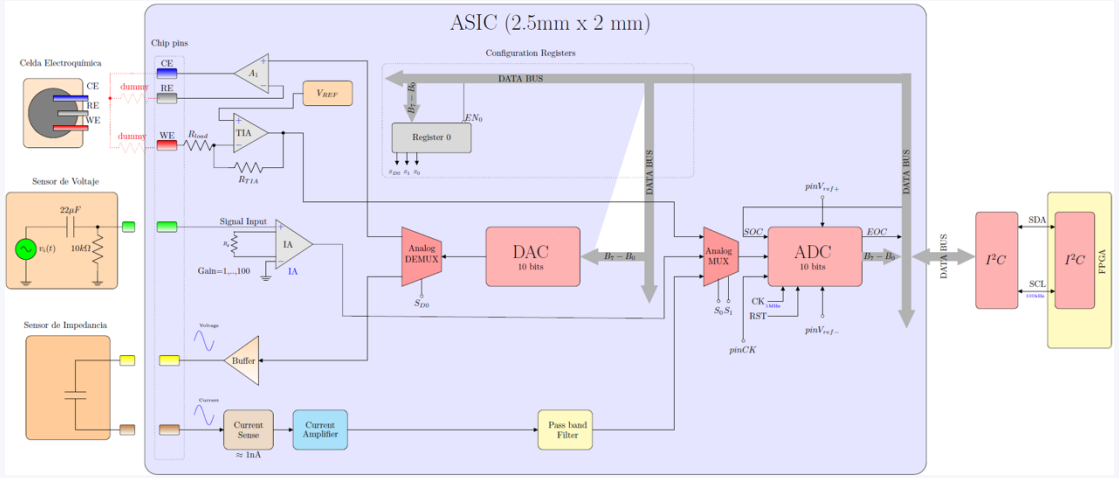
We focus on analog, mixed-mode, RF and digital design for the automotive, medical equipment, and household appliances.



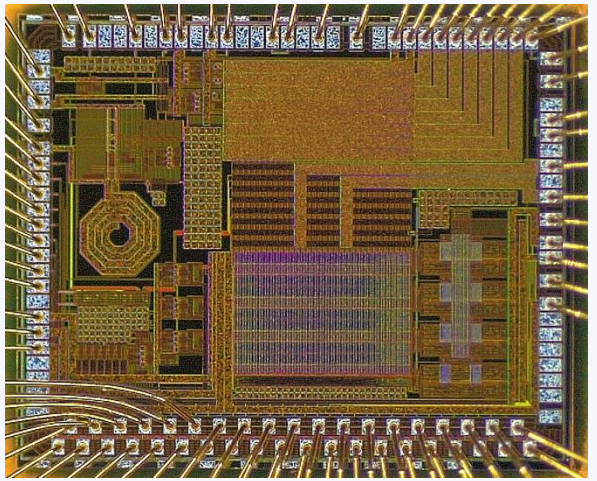
* With the support of the State Governments of Jalisco, Puebla, and Sonora.

From the concept to the silicon chip and testing

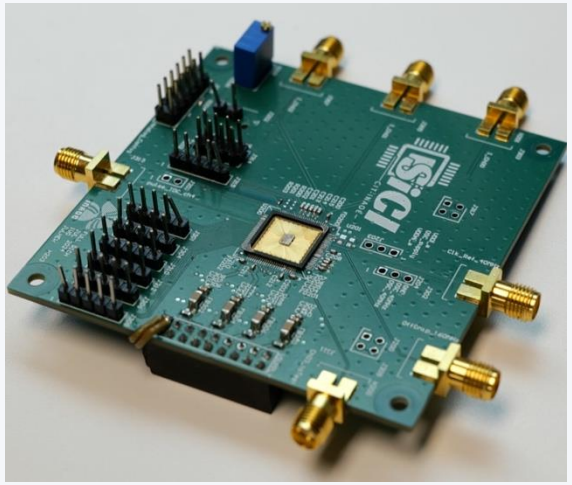
Concept and client specs



Layout, IC design & simulation



Prototyping & testing



We work under the concept of fabless and tape out to manufacture in 180 nm, 65 nm, 22 nm, or 16 nm

The articulated model

Academic partners

Human resources
+
Workforce development

Innovation liaison (IBdMX)

INNOVA BIENESTAR
INNOVACIÓN SOBERANA PARA EL BIENESTAR

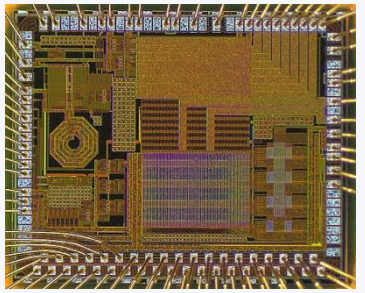
Kutsari Semiconductors

Investor & Gov. partners

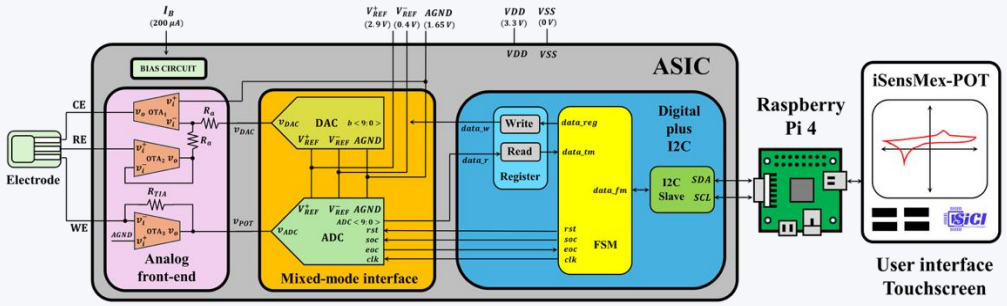
Jalisco
Puebla
Sonora

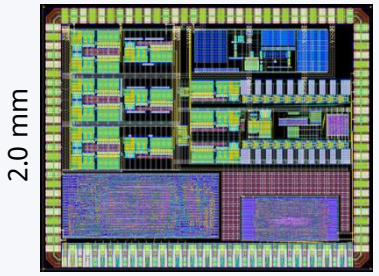
Industry partners

Product/Customer



Sample gallery of the latest IC designs

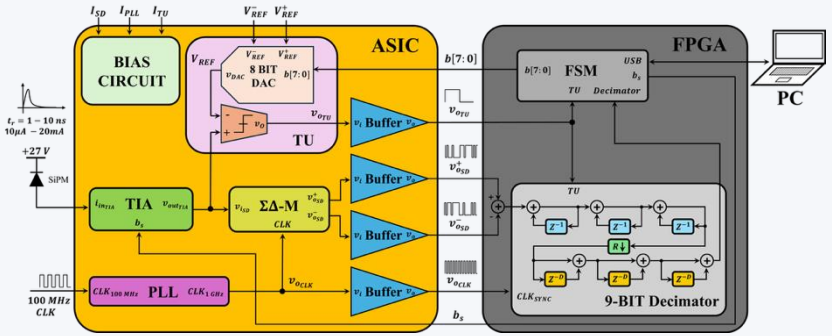


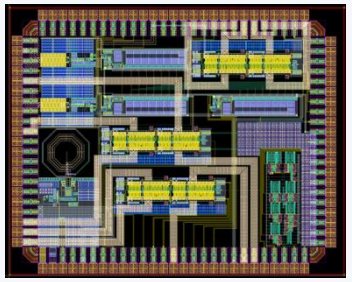


1 “Tonantzin”

TSMC 180 nm, 5mm², QFN100
- Analog front-end
- 10 bit ADC/DAC
- Internal biasing
- I²C protocol
- Customer: medical device

Application:
Creatinine detection system for early prediction of degenerative kidney disease.

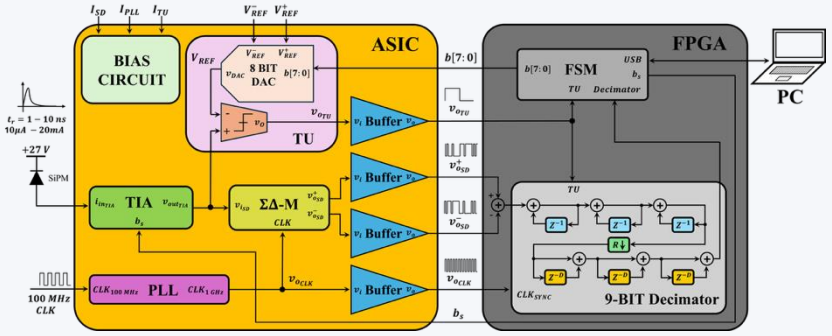


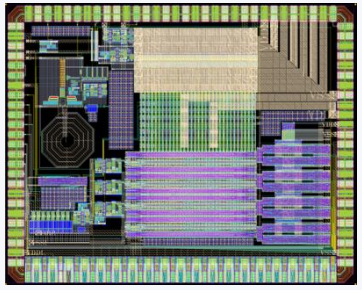


2 “MexSiC”

TSMC 180 nm, 5mm², QFN100
- Mixed mode front-end
- Sigma delta (ΣΔ-M) modulator
- Internal biasing
- I²C protocol
- PLL
- Trigger unit
- Customer: Nuclear Sc. Inst. UNAM

Application:
Data acquisition channel (DAQ) designed for silicon photomultipliers (SiPM).





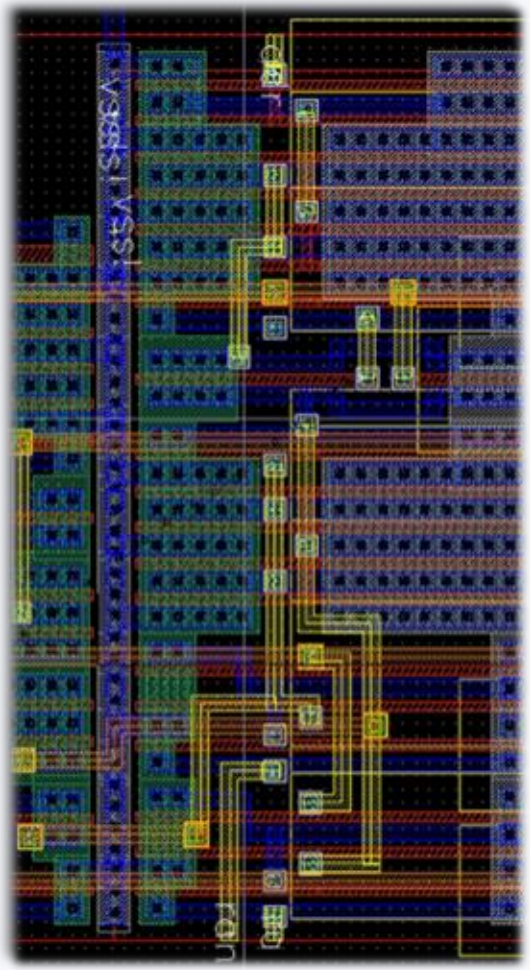
3- “MexSiC-TDC”

TSMC 180 nm, 5mm², QFN100
- Analog front-end
- A 48.8 ps Time-to-Digital converter
- Internal biasing
- I²C protocol
- PLL
- Customer: NSI UNAM/ALICE CERN

Application:
The analog front-end converts the current delivered by the SiPM into a voltage using a @ 100 MHz transimpedance amplifier.

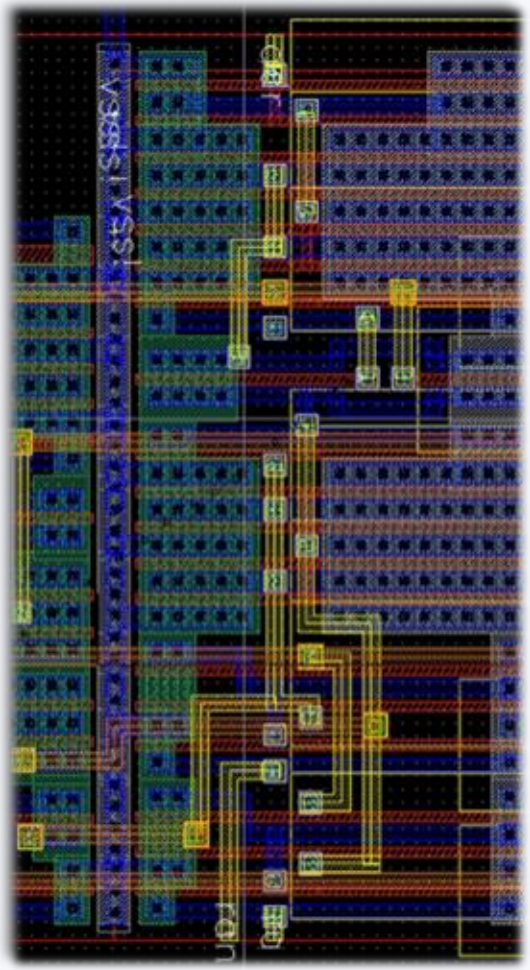
Who are we?

- A group of designeers with more than 20 years of experience recruited from the academia and industry.
- We are located in Mexico with offices in the states of Puebla, Jalisco, and Sonora.
- We train designers through a specialized 6-months program with hands on design tools, and fabrication of a test chip.

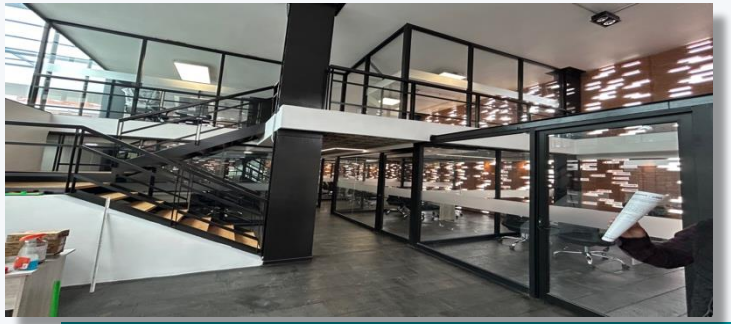


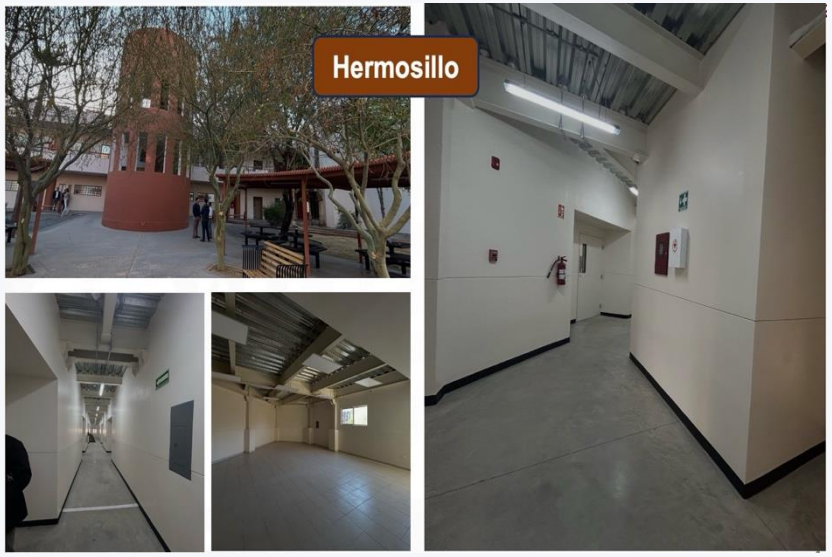
We aim at

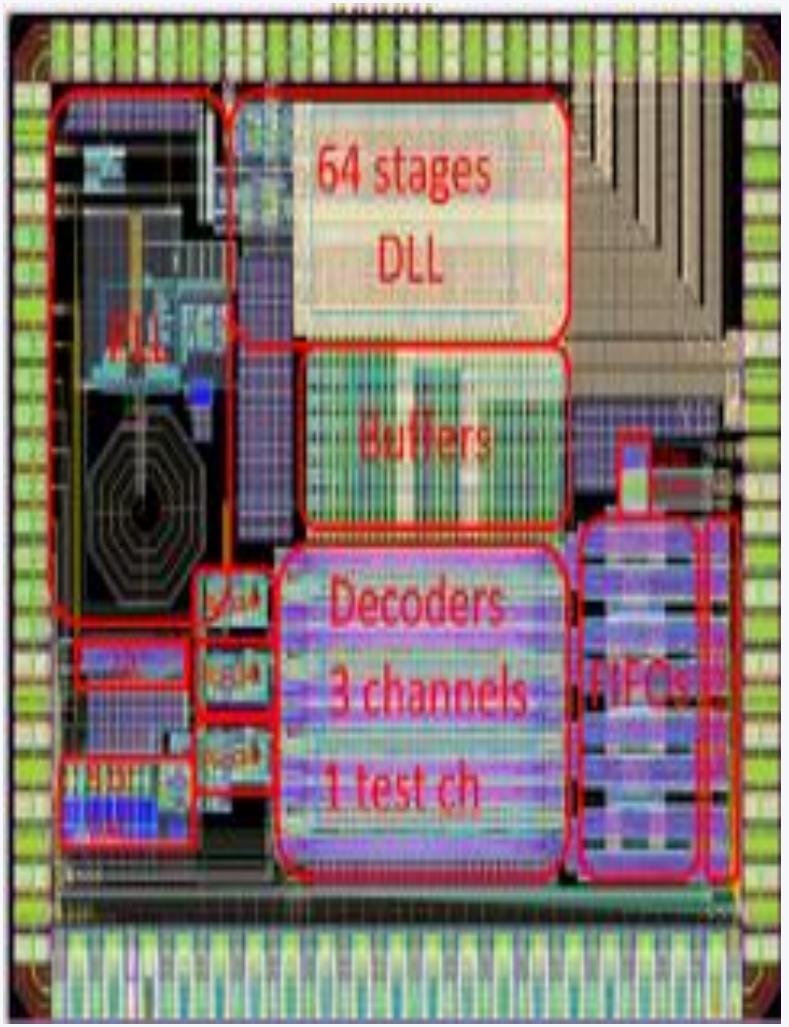
- Setting up a 100 IC designers design house by 2027.
- Strengtegning the Academia-Industry collaboration.
- Achieving economic self-sustainability by 2028.
- Cross-collaboration for the design of ICs.
- Establish the conditions for the installation of a semiconductor factory by 2030.



Our offices in Puebla, Jalisco, and Sonora.







Leadership Team & Contact

Credible leadership and an execution-focused technical bench

Dr. Edmundo Gutiérrez
General head

PhD, Catholic University of Leuven, Belgium, 1993.
https://scholar.google.com/citations?hl=es&user=eRQRMb8AAAAJ

A technical group of 18 designers with a PhD in circuit synthesis and design, analog and digital signal processing, IoT security, analog/RF and mixed signal, low-power systems, 5G and wireless communications, ASIC, SoC design, FPGA embedded systems, readout circuits, scientific instrument development, Analog-to-Digital and Digital-to-Analog converters, medical and environmental oriented applications, graphic interfaces for ASIC controlling, design and characterization of image arrays, ESD protection, signal integrity, and reliability at room and cryogenic temperatures. We have designed in different technologies, such as 16 nm, 65 nm, and 180 nm CMOS, and tested 14nm FinFET technology for reliability modeling.

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